

DECLARATION

I, NOBUMITSU ASAHI, a Japanese Patent Attorney registered No. 10435, of Okabe International Patent Office at No. 602, Fuji Bldg., 2-3, Marunouchi 3-chome, Chiyoda-ku, Tokyo, Japan, hereby declare that I have a thorough knowledge of Japanese and English languages, and that the attached pages contain a correct translation into English of the priority documents of Japanese Patent Application No. 2003-061288 filed on March 7, 2003 in the name of CANON KABUSHIKI KAISHA.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made, are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signed this 19th day of August, 2008



NOBUMITSU ASAHI

PATENT OFFICE
JAPANESE GOVERNMENT

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Applicant's Information

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[Name of the Document] Specification

[Title of the Invention] EL Panel

[What is Claimed is]

[Claim 1]

An EL panel at least including:

an image display unit in which a plurality of pixel units including EL elements for emitting light in response to a current signal are arranged in a matrix; and

a column control unit in which voltage-current conversion circuits for converting a single or plurality of voltage signals to a single current signal are arranged corresponding to the number of the columns of said pixels unit to supply said current signal to a pixel unit of the corresponding column,

said EL panel further comprising:

a total sum current detection unit consisting of:

a total sum current output unit for outputting the total sum current of a current flowing through a column information line group comprising column information lines for connecting the voltage-current conversion circuit to the pixel unit of the corresponding column to the outside; and

an interception unit for intercepting a

current flowing through a column information line of said total sum current output unit on said image display unit side.

[Detailed Description of the Invention]

[0001]

[Field of the Industrial Utilization]

The present invention relates to an EL panel using an electroluminescence element (hereinafter called an EL element) which emits light due to current injection for image display. The present invention particularly relates to a technology for conducting tests of a drive circuit easily.

[0002]

[Prior Art]

An EL panel is applied to a panel type image display system (hereinafter called an EL panel). In the EL panel, a current setting system is generally employed as a light emission control system of each pixel.

[0003]

A schematic diagram for showing the configuration of a color EL panel of the conventional current setting system is shown in FIG. 6. In FIG. 6, pixel units 8 including EL elements of the respective colors in charge of image display of the three primary colors are two-dimensionally arranged in N columns and M rows so as to constitute an image

display unit 9. An image signal VIDEO including the information on the three primary colors is supplied to a column control unit 5 which is comprised of N column control circuits. The column control circuits are arranged to be corresponding to the three primary colors, respectively.

[0004]

A video sampling signal group SP which is generated by transiting at every one period or at every half period of a column scanning clock KC by a column scanning start signal SPC is output from a column shift register 4 to which the column scanning clock KC is input and input into the corresponding column control circuit.

[0005]

The video signal VIDEO for a predetermined period is sampled in each column control circuit, and a current signal corresponding to the column information line group data is output to be input to an image unit 8 of the corresponding column.

[0006]

A column control signal SC is input to a logic circuit 6, and the column control signal is input to the column control unit 5 through the column control line group 7.

[0007]

On the other hand, each row control signal

which is generated by transiting at every one period or at every half period of a column scanning clock KR is output from a column shift register 4 to which a row scanning clock KR is input by a column scanning start signal SPR and input into the pixel unit 8 of the corresponding row through a row control line group 11.

[0008]

The column control unit 5 is arranged to convert a point sequential voltage image input signal into a line sequential current image signal in rows, and can be arranged in an analog system or a digital system.

[0009]

FIG. 11 shows a circuit diagram illustrating a configuration example of column control circuit in an analog system having a simple circuit configuration. Three of the unit shown in FIG. 11 make a set for the three primary colors. A voltage image signal VIDEO of a corresponding color is input to a sample hold circuit SH. On the other hand, a control signal is connected to the column shift register 4 from the logic circuit 6, and sampling pulses PSa and SPb of the corresponding column which are generated in each odd and even row periods are input into the sampling circuit SH. Further, row control signals CC3 and CC6 which serve as the row

control line group 11 are also connected to the sample hold circuit SH. An output voltage signal v (data) of sample hold circuit SH is input to a voltage-current conversion circuit gm, so as to output a current signal data. A bias signal VB and a column control signal CC7 as the column control line group 7 are connected to the voltage-current conversion circuit gm.

[0010]

An operation in FIG. 11 will be described with reference to a time chart of FIG. 12. A voltage image signal VIDEO is input with a correlation with a reference signal REF.

[0011]

In a period T1 which is a row period, a column control signal CC3 reaches the L level (a column control signal CC6 reaches the H level), while the sampling pulse SPa is output (SPb is not output), and the voltage image signal VIDEO is sample-held in the sample hold circuit SH with a difference voltage d1 from the reference signal REF in the generation period t1 of the sampling pulse Pa of the corresponding column, as shown in the diagram.

[0012]

In a period T2 which is a row period, the column control signal CC3 reaches the H level (the column control signal CC6 reaches the L level), so

that the VIDEO signal which is sample-held by the voltage signal v (data) in the period $T1$ is output, while the sampling pulse SPb is output (the sampling pulse SPA is not output), and the voltage image signal VIDEO is sample-held in the sample hold circuit SH with a difference voltage $d2$ from the reference signal REF in the generation period $T2$ of the sampling pulse SPb of the corresponding column, as shown in the diagram.

[0013]

In a period $T3$ which is a row period, the column control signal $CC3$ becomes the L level for the second time (the column control signal $CC6$ becomes the H level), and the VIDEO signal which is sample-held by the voltage signal v (data) in the period $T2$ is output.

<Description of the voltage-current conversion circuit>

The voltage-current conversion circuit gm is arranged to output a current signal data with a correlation with difference voltages $d1$, $d2$, $d3$... with respect to the reference signal REF . The difference voltage $d1$ held in the period $T1$ is converted into a current $I (m)$ in the period $T2$, the difference voltage $d2$ held in the period $T1$ is converted into a current $I (m+1)$ in the period $T3$, and then the difference voltage $d2$ held in the

preceding period is converted into a current $I_{(m-1)}$ in the period T_1 . These currents are output in the respective periods.

[0014]

FIG. 10 is a diagram showing the configure of the voltage/current circuit gm. In FIG. 10, a transistor M6 is turned off only when the current supply to the pixel unit 8 must be stopped, i.e., at the power supply starting time or at a waiting time, and the transistor M6 is normally in an ON state during operation owing to the column control signal CC7. This is a circuit configuration generally known so that the detailed description thereof will be omitted. Note that M2, M4 and Mr characteristically have correlativity with M3, M5 and M1, respectively. The conversion characteristics can be set by an M1/D current and a drive coefficient β of M2 and M3.

[0015]

The column control circuit described above adopts an analog system. When a digital system circuit is used, the reference signal REF becomes unnecessary, the voltage image signal becomes a plurality of data signals, and the sample hold circuit SH becomes a master slave type flip-flop group for holding each data signal, so as to outputs plural pieces of voltage output data $v_{(data)}$. The voltage-current conversion circuit gm becomes a

current-output type DA conversion circuit based on a weighted current corresponding to each data for determining a gm characteristic.

[0016]

<Description of pixel unit>

FIG. 8 is a circuit diagram for showing a circuit configuration example of a pixel unit 8 of a current programming type. In the configuration shown in FIG. 8, three circuits are provided in the pixel unit 8, each for driving an EL element of each color.

[0017]

A column information line data of the corresponding column is connected to an M4/S, a row signal line RC1 of the corresponding row is connected to an M4/G, and an M4/D is connected to an M2/D as well as an M3/D. An M2/S is connected to the power supply voltage VCC, an M2/G is connected to a capacity C1, one end of which is connected to the power supply voltage VCC, and an M1/S and M3/S. An M3/G is connected to a row signal line RC2 of the corresponding row. An M1/S is connected to the power supply voltage VCC and an M1/D is input to a current injection terminal of the EL element, and the other end of the EL element is grounded (GND).

[0018]

An operation of the pixel unit 8 will be described with reference to a time chart of FIG. 9.

A current image signal of a corresponding column is input into the information line data of the corresponding column, being updated every row period.
[0019]

At a time t_0 , when a row control signal RC_1 of a corresponding row reaches the H level and a row control signal RC_2 reaches the L level, a voltage of the M_2/G according to the current drive ability of the transistor M_2 is generated by a current image signal $I(m)$ at that point of time, and the capacity C_1 is charged. When the sizes of the transistors M_2 and M_1 are set relatively to each other, a current proportional to the current image signal $I(m)$ is output to the M_1/D . At a time t_1 , the row control signal RC_2 changes to the H level, and the transistor M_3 is turned off. Thereby, the voltage of the M_2/G is held. At a time t_2 , the row control signal RC_1 changes to the H level, and the corresponding pixel unit 8 is separated from the current image signal. Then, the transistor M_4 supplies a current proportional to the set current image signal $I(m)$ to the corresponding EL element continuously until the transistor M_4 is turned on next.

[0020]

FIG. 7 is a circuit diagram for showing another circuit configuration example of the pixel unit 8 of the current programming type. In the

configuration of FIG. 7, three circuits are provided in the pixel unit 8, in the same manner as in FIG. 8, each for driving an EL element of each color.

[0021]

A column information line data of a corresponding column is connected to an M3/S, a row signal line RC1 of the corresponding row is connected to an M3/G, an M3/D is connected to an M2/D as well as an M4/S, and an M4/G is also connected to the row signal line RC1. An M1/S is connected to the power supply voltage VCC, an M1/G is connected to the capacity C1, one end of which is connected to the power supply voltage VCC, and M2/S, and an M2/G is connected to a row signal line RC2 of the corresponding row. An M4/D is input to a current injection terminal of the EL element, and the other end of the EL element is grounded (GND).

[0022]

An operation of the pixel unit 8 will be described with reference to a time chart of FIG. 9. A current image signal of a corresponding column is input into the information line data of the corresponding column, being updated every row period.

[0023]

At a time t0, when the row control signal RC1 of the corresponding row reaches the H level and the row control signal RC2 reaches the L level, a voltage

of the M1/G according to the current drive ability of the transistor M1 is generated by a current image signal $I(m)$ at that point of time, and the capacity C1 is charged. However, at this time, the transistor M4 is off, and no currents is injected into the EL element. At a time t1, the row control signal RC2 changes to the H level, and the transistor M2 is turned off. Thereby, the voltage of the M1/G is held. At a time t2, the row control signal RC1 changes to the L level, and the transistor M4 is turned on, and the current held by the transistor M1 is injected into the EL element, meanwhile the corresponding pixel unit 8 is separated from the current image signal. Then, the transistor M4 supplies a current proportional to the set current image signal $I(m)$ to the corresponding EL element continuously until the transistor M3 is turned on next.

[0024]

[Problems to be Solved by the Invention]

However, the EL panel shown in FIG. 6 has the following problems.

[0025]

(Problem 1)

The circuits for the EL panel described above are constituted of thin film transistors(TFTs). In a TFT, it is difficult to securely obtain the correlativity of the transistor characteristics.

Therefore, it is difficult to regulate conversion characteristics of the voltage-current conversion circuit gm which are important for column control signal generation of the analog system shown in FIG. 10 for each column, which may generate "vertical stripes" on a reproduced image due to the dispersion of current signals for each column, thereby causing deterioration in the image quality. In the current-output type DA conversion circuit of the digital system, it is also difficult to securely obtain relative precision between weighted current supply sources incorporated in each of the circuits, which may also cause the dispersion of the current signals for each column to generate "vertical stripes" on a reproduced image, thus resulting deterioration in the image quality.

[0026]

(Problem 2)

For the EL panel, EL elements are generally formed after formation of TFT circuits. To this end, it is important for the cost reduction of the EL panel to find any defect of the TFT circuits having a great number of pixel units, before forming the EL elements. However, for the EL panel having the configuration of FIG 6, it is impossible to conduct prior check of the TFT circuit operation of the pixel unit quickly and in a non-contact manner.

[0027]

The present invention has been contrived taking the above-described problems into consideration, and an object thereof is to provide an EL panel in which voltage-current conversion characteristics of a column control unit can be detected in an arbitrary column area, and further, the operational characteristics of a pixel unit of each row in an arbitrary column area can be confirmed without contacting an electrode of the pixel unit.

[0028]

[Means for Solving the Problems]

(Solving means 1)

An EL panel at least including:

an image display unit in which a plurality of pixel units including EL elements for emitting light in response to a current signal are arranged in a matrix; and

a column control unit in which voltage-current conversion circuits for converting a single or plurality of voltage signals to a single current signal are arranged corresponding to the number of the columns of the pixel units to supply the current signal to a pixel unit of the corresponding column,

characterized by further comprising:

a total sum current detection unit consisting of:

a total sum current output unit for outputting the total sum current of a current flowing through a column information line group comprising column information lines for connecting the voltage-current conversion circuit to the pixel unit of the corresponding column to the outside; and

an interception unit for intercepting a current flowing through a column information line of said total sum current output unit on said image display unit side.

[0029]

(Solving means 2)

The EL panel set forth in the above solving means 1, characterized in that the total sum current output unit is comprised of a group of output switches which connect each column information line to a total sum current output line and are capable of opening and/or closing control.

[0030]

(Solving means 3)

The EL panel set forth in the above solving means 1 or 2, characterized in that the interception unit is comprised of a group of output switches which are connected to the respective column information lines between the total sum current output unit and the image display unit and are capable of opening and/or closing control.

[0031]

(Solving means 4)

An EL panel at least including:

an image display unit in which a plurality of pixel units including EL elements for emitting light in response to a current signal are arranged in a matrix; and

a column control unit in which voltage-current conversion circuits for converting a single or plurality of voltage signals to a single current signal are arranged corresponding to the number of the columns of the pixel units to supply the current signal to a pixel unit of the corresponding column,

characterized by being capable of intercepting an input of a current signal from the column control unit to the pixel unit and outputting the total sum current of a current signal group from the column control unit to the outside.

[0032]

(Solving means 5)

An EL panel at least including:

an image display unit in which a plurality of pixel units including EL elements for emitting light in response to a current signal are arranged in a matrix; and

a column control unit in which voltage-current conversion circuits for converting a single

or plurality of voltage signals to a single current signal are arranged corresponding to the number of the columns of the pixel units to supply the current signal to a pixel unit of the corresponding column,

characterized by being capable of supplying a current signal of each column of the column control unit to the pixel unit of each column, intercepting an output of the column control unit after generating a drive set current of the EL element in the pixel unit of a selected row and then storing a value of the drive set current, and then outputting the total sum current of the drive set current group to the outside.

[0033]

[Description of the Preferred Embodiments]

Embodiments of an EL panel according to the present invention will be described below with reference to the drawings. However, the present invention is not limited to these embodiments. In the EL panel of the present invention, arrangements and operations other than those specifically described in the following are the same as the arrangements and operations described in the prior art.

[0034]

In the present specification, a gate electrode, a source electrode and a drain electrode

of a transistor are denoted by the abbreviations of /G, /S and /D, respectively, for the sake of convenience of the description. A signal and a signal line for supplying the signal may be expressed as the same symbol without special discrimination.

[0035]

(Embodiment 1)

FIG. 1 is a schematic diagram for showing the EL panel of the present invention, which is different from the conventional EL panel shown in FIG. 6 mainly in that a total sum current detection unit 1 is additionally provided between the column control unit 5 and the image display unit 9.

[0036]

A test signal TEST is input to logic circuits 2 and 6, and a total sum current detection control signal 3 is input to the total sum current detection unit 1 from the logic circuit 2. A total sum current is output from the total sum current detection unit 1 through a total sum current output line Iout.

[0037]

FIG. 2 shows a circuit configuration example of the total sum current detection unit 1. The total sum current detection unit of the present embodiment consists of a total sum current output unit 1a and an interception unit 1b. The total sum current output unit 1a consists of a group of output switches (Min

to M3n) which connect each column information line (data (na) to data (nc)) to the total sum current output line Iout and are capable of opening/closing control, while the interception unit 1b consists of a group of interception switches (M4n to M6n) which are connected to the respective column information lines between the total sum current output unit 1a and the image display unit 9 and are capable of opening/closing control (n denotes the number of the RGB set).

[0038]

Connection manners will be described below more detailedly. The column information lines for connecting the voltage-current conversion circuit and a pixel unit of a corresponding column are connected through the M1n/S to M6n/S, and all of the M1n/D, M2n/D and M3n/D are connected to each other so as to output the total sum current from the total sum output line Iout. On the other hand, the M4n/D, M5/D and M6/D are connected to the column information lines data (na), data (nb) and data (nc) of the corresponding column. All of the M1n/G, M2n/G and M3n/G (M4n/G, M5n/G and M6n/G) are connected to each other so that a detection control signal CCx (CCy) (the total sum current detection control signal 3) which is an output of the logic circuit 2 is connected thereto.

[0039]

It should be noted that all of the transistors are arranged to perform switching operation, and by controlling appropriately, their types being n-types or p-types and their configurations are not limited.

[0040]

The pixel unit 8 may take either the configuration shown in FIG. 7 or that in FIG. 8.

[0041]

A detection operation of an output current of the column control unit 5 in the EL panel in FIG. 1 will be described with reference to a time chart in FIG. 3. Note that the column control circuits shown in FIG. 11 are supposed to be in the state of outputting currents by the column control signal CC7.

[0042]

For detecting output currents of the column control units, all of the M1n, M2n and M3n are turned on and all of the M4n, M5n and M6n are turned off. That is, in the total sum current detection unit 1, all of the M1n, M2n and M3n are turned on by the detection control signal CCx and all of the M4n, M5n and M6n are turned off by the detection control signal CCy so that all of the column control currents output from the column control unit 5 can be output to the total sum current output line Iout as a total

sum current.

[0043]

Also in this state, as shown in FIG. 3, the timings of the pulses SPa and SPb, and signals CC3 and CC6 are the same as those of the normal operation shown in FIG. 12. However, the image signal VIDEO is set in a level on which the signal is generated only in the areas $Z(n-1)$ to $Z(n+6)$ which are different in each row period and an output current of the column control circuit becomes smaller in an area other than the corresponding area. When the column control circuit employs the digital system, all of the image data VIDEO is set to be (0) in an area other than those described above.

[0044]

With this, a total sum current $\Sigma I(n)$ having an output current from a column control circuit corresponding to the area $Z(n)$ in the row period T_1 as a main component is output from the total sum current output line I_{out} in the row period T_2 . Also in other periods, a total sum current having an output current from a column control circuit in a corresponding area as a main component is output from the total sum current line I_{out} .

[0045]

If the above area group is set to include an effective image period, the output currents from all

of the column control circuits can be confirmed. On the other hand, if each area $Z(n)$ is set to be corresponding to one column (single color), output currents from all of the column control circuits can be individually detected. Further, if each area is set to be corresponding to appropriate plural numbers of the columns in accordance with the dispersion of TFT characteristics, the detection time of the output currents of all the column control circuits can be reduced, and moreover, the dispersion of TFT characteristics which must be visually noticed can be extracted. Furthermore, the areas may be overlapped to one another, and the order of the areas are not limited.

[0046]

As described above, output currents from the column control circuit group can be detected in any area and, if an image signal (image data) VIDEO is corrected based on a result of this detection and is input, it is rendered possible to negate the dispersion of TFT characteristics easily in a short period of operation activation.

[0047]

(Embodiment 2)

In this second embodiment, an EL panel to be used is the same as that shown in the first embodiment.

[0048]

This embodiment is arranged to detect a drive set current for setting a drive current for driving an EL element included in the pixel unit 8, and an operation thereof will be described with reference to a time chart shown in FIG. 4.

[0049]

It should be noted that, all of the transistors of the M4n, M5n and M6n (the interception unit 1b) in the total sum current detection unit in FIG. 2 are turned on by the detection control signal CCy. That is, the interception unit 1b is in an open state. In addition, a generation area Z(n) of an image signal VIDEO is fixed in a predetermined period.

[0050]

In the period T1, a sampling pulse Spa is generated, and an image signal VIDEO is current-converted in the corresponding column control unit 5. In the period T2, the signals change to CC7=H and CCx=L level, and, in the pixel unit 8 corresponding to the m-th row which is selected by m-th row control signals RC1(m) and RC2(m), in the same manner as in a normal operation, a drive set current of the EL element is caused to generate and a value of the drive set current is stored. In the period T3, the signals change to CC7=L and CCx=H level, and the column control unit 5 does not output a current signal to

each column information line data. Moreover, since the row control signal RC2(m) changes to the H level, the drive set current Id which is held in each pixel unit 8 of the m-th row is supplied to each column information line data, and the total sum current Id(m) of the drive set current of the m-th row is output to the total sum current output line Iout.

[0051]

In the same manner, due to a current signal converted by the sampling pulse SPb in the period T3, a total sum current $\Sigma Id(m+1)$ of the EL drive current of each pixel unit 8 of the (m+1)th row is output to the total sum current output line Iout in the period T5.

[0052]

Thus, according to this embodiment, a current signal of each column of a column control unit is supplied to a pixel unit of each column, and a drive set current of an EL element is caused to generate in the pixel unit of the selected row, so that, after a value of the drive set current is stored, an output from the column control unit is intercepted and the total sum current of the drive set current group is output from the total sum current output unit to the outside. Thus, the operational characteristics of a pixel unit of each row in an arbitrary column area can be confirmed in a non-contact manner with respect

to an electrode of the pixel unit. In this case, by fixing the area $Z(n)$ as shown in FIG. 4, it is possible to sequentially detect a drive current of the pixel unit 8 in the corresponding column area.

[0053]

(Embodiment 3)

Also in this embodiment, an EL panel to be used is the same as that shown in the first embodiment. This embodiment is the same as the second embodiment in that a drive set current for setting a drive current for driving an EL element included in the pixel unit 8 is to be detected.

[0054]

This embodiment is different from the second embodiment in that in the generation periods of the respective sampling pulses, the areas $Z(n)$, areas $Z(n+1)$, areas $Z(n+2)$ and areas $Z(n+3)$ are respectively set in the same areas, the areas are set differently for each of the groups, and an EL drive current in a set column area can be confirmed in accordance with the detected total sum drive current of each of the rows $\Sigma I_d(m-1)$ to $\Sigma I_d(m+2)$.

[0055]

It is also possible to check a TFT circuit operation effectively in the EL panel including a number of pixel units 8 by setting a detection area Z for each purpose, in the same manner as in the second

and third embodiments.

[0056]

[Effect of the Invention]

As described above, according to the EL panel of the present invention, it is possible to detect the voltage-current conversion characteristics of a column control unit in an arbitrary column area only by additionally providing the total sum current detection unit having a very simple configuration and then to correct the characteristic dispersion of the column control by using this. It is also possible to confirm the operational characteristics of a pixel unit of each row in an arbitrary column area without contacting an electrode of the pixel unit.

[Brief Description of the Drawings]

[FIGURE 1]

A schematic diagram for showing the EL panel of the present invention.

[FIGURE 2]

A circuit diagram for showing an embodiment of the total sum current detection unit which is provided in the EL panel of the present invention.

[FIGURE 3]

A time chart for explaining Example 1.

[FIGURE 4]

A time chart for explaining Example 2.

[FIGURE 5]

A time chart for explaining Example 3.

[FIGURE 6]

A schematic diagram for showing the configuration of the conventional EL panel.

[FIGURE 7]

A circuit diagram for showing a circuit configuration example of the pixel unit.

[FIGURE 8]

A circuit diagram for showing another circuit configuration example of the pixel unit.

[FIGURE 9]

A time chart for explaining an operation of the pixel unit having the circuit configuration of FIG. 7 or FIG. 8.

[FIGURE 10]

A circuit diagram for showing a configuration example of the voltage-current conversion circuit.

[FIGURE 11]

A circuit diagram for showing a configuration example of the column control circuit.

[FIGURE 12]

A time chart for explaining an operation of the column control circuit having the circuit configuration shown in FIG. 11.

[Description of Reference Numerals or Symbols]

1 ... total sum current detection unit

1a ... total sum current output unit

1b ... interception unit
2 ... logic circuit
3 ... detection control line
4 ... column shift register
5 ... column control unit
6 ... logic circuit
7 ... column control line
8 ... pixel unit
9 ... image display unit
10 ... row shift register
11 ... row control signal line

[Name of the Document] **Abstract**

[Abstract]

[Object]

An object of the present invention is to provide an EL panel in which voltage-current conversion characteristics of a column control unit which conducts a voltage-current converting operation can be detected in an arbitrary column area, and further, the operational characteristics of a pixel unit of each row in an arbitrary column area can be confirmed without contacting an electrode of the pixel unit.

[Means for Achieving the Object]

Disclosed is an EL panel at least including an image display unit 9 in which a plurality of pixel units 8 including EL elements are arranged in a matrix and a column control unit 5 in which voltage-current conversion circuits are arranged corresponding to the number of the columns of the pixel units 8 to supply the current signal to a pixel unit 8 of the corresponding column, characterized by further comprising a total sum current detection unit consisting of a total sum current output unit for outputting the total sum current of a current flowing through a column information line group comprising column information lines data for connecting the voltage-current conversion circuit to the pixel unit

8 of the corresponding column to the outside and an interception unit for intercepting a current flowing through a column information line of the total sum current output unit on said image display unit side.

[Elected Drawing]

FIGURE 1